Agilent Technologies ParBERT 81250 Mux/Demux Application

Application Note

Agilent Technologies

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Mux/Demux is an important part of communication. They are responsible for transmitting information, either electrical or optical, on one data link. On the transmitter side (TX), the information is collected and put on one line with speeds of 4, 7, 10 or 20 times faster than on the parallel side, with the help from the MUX circuitry. On the receiver side (RX), the DEMUX circuitry will receive the high-speed data and converts it to a parallel bus so that following protocol Asics can process it. Figure 1 is an example of a 1:4 implementation, thus, the frequency on the serial side is 4 times faster.
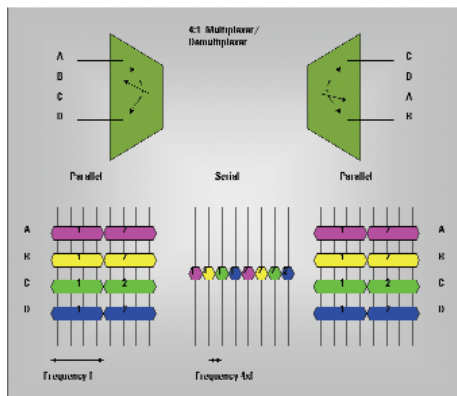
The areas for using such parts are:
• Local Area Networks
• Digital Video
• Global Networks

Within the Local Area Networks, the applications are:
• Gigabit Ethernet
• Fiber Channel
• Storage Area Networks

These applications work with a serial speed of 2.5 Gbit/s and the MUX ration is typically 1:10.

The Digital Video applications are:
• HDTV
• Display Links
• Flat Panel Interface

Here the serial speed is at present up to 1.5 Gbit/s and the typical MUX ratio is 1:7. The total bandwidth of such a link is often much higher, but this results in having several lines combined.

The global networks are terrestrial or undersea with SONET/SDH protocol. Here the serial speeds are 10 Gbit/s but in future could possibly reach 40 Gbit/. The MUX ratio is 1:4 and 1:16.

Display Link

There are single silicon CMOS integrated circuits. This application note refers to National's DS90C387. The chips come in a 100-pin PQFP package. The serializer and de-serializer come in independent packages. The total bandwidth is up to 5.38 Gbit/s, but this is achieved using up to 8 serial lines. Every serializer/de-serializer uses 7 parallel lines to achieve a total of 48 RGB data signals. The serial lines work with LVDS technology.
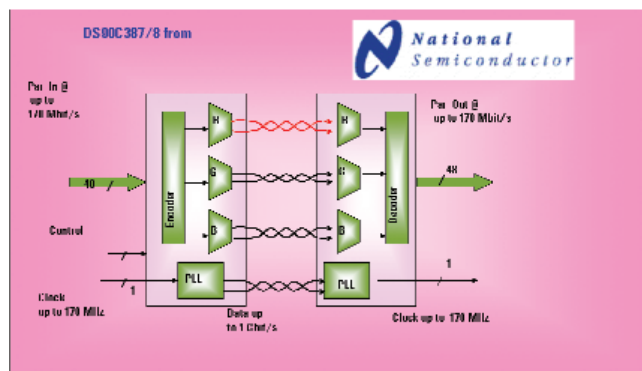

Figure 1: Mux/Demux Application

Figure 2: Mux/Demux Application

Gigabit Ethernet/Fiber Channel Implementation

There are single silicon bipolar integrated transceivers available on the market from several vendors. This application note reflects on Agilent's HDMP-263x chip. This chip comes in a 64-pin QFP package, as a low cost physical layer solution. The serializer and de-serializer are both in one package. The parallel side is 10 bit wide for 8B/10B coding. The receiver synchronizes the 'comma' character.

10 Gbit/s Transceiver

This refers to a chipset provided by GIGA. There are two silicon bipolar integrated circuits for TX and RX. They are housed in 68-pin multi-layer ceramic packages. The 10 Gbit/s are used with SONET OC-192 and SDH STM-64. The parallel side is 16-bit wide and operating at 622 MHz.

The points of interest for the designer concerning these three areas are the timing parameters:

- Parallel Data to Clock (setup- /hold time)
- Parallel to Serial Data (latency)
- Clock Duty Cycle
- Supply Voltage tolerance
- Input sensitivity, Output signal (Eye diagram)
- Jitter (serial out).

For measurement on the serial side of the 10 Gbit tranceiver, the equipment required must be able to cope with the 10 Gbit/s speed.

PRBS/PRWS Data Needs

For testing the physical layer, the industry has established the 'Pseudo Random Binary Sequence' (PRBS). This is standardized by IEEE/ITU. It is defined by the polynom 2^n-1 and algorithm. It provides well-defined stress to the device under test (DUT) by defining the maximum number of consecutive 1's and 0's.

The data stream is predicatable as by capturing nbit without failure, you can predict future signals. So a receiver can be synchronized for BER measurement out of running data stream. There is no need to know the start or synchronization signal from the stimulating side.

Figure 3: Agilent's HDMP-263 x block diagram

Figure 4: 10 Gbit/s transceiver

Pseudo Random Word Sequence (PRWS) is defined by:
- Polynom 2^n-1
- Algorithm
- Parallel bus width

The bits of the PRBS will be assigned to the parallel lines the way that after multiplexing together it is a PRBS

Synchronization Needs

As the latency from parallel to serial side (or vice versa) may not be known or it is unpredictable, as it changes at every power up, the synchronization of incoming data can be performed before the BER measurement can take place. For synchronization there are two principles:
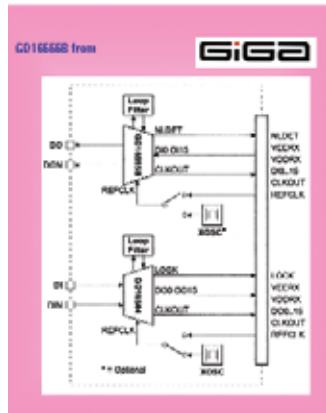- data
- sampling point delay adjust
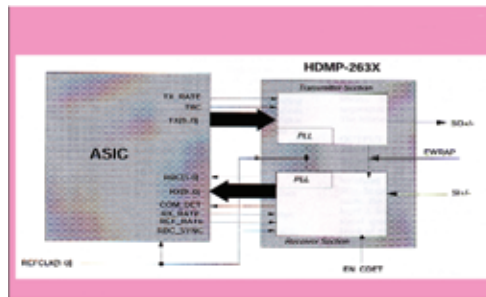
It is impossible to generate a PRWS for every polynomial and port width combination. The table given shows the restrictions. Good polynoms are 2^7-1 and $2^{31}-1$ as there are no limitations on up to 64 port sizes.

Polynomia	Invalid port-widths
2^5-1	31, 62
2^6-1	3,7,9,18,21,27,36,42,54,63
2^8-1	3, 5, 15, 17, 34, 51
2^9-1	7
2^10-1	3, 11, 31, 33
2^11-1	23
2^12-1	7,9,13,15,21,35,45, 63
2^14-1	3, 43
2^15-1	7, 31
2^23-1	47

The first principle shifts the expected data cycle by cycle, until it matches with the incoming data. This is possible in an unrestricted range, with PRBS especially as there is a register, which is loaded firstly with part of incoming stream and then continues to generate further streams. This is possible due to the specific nature of PRBS.
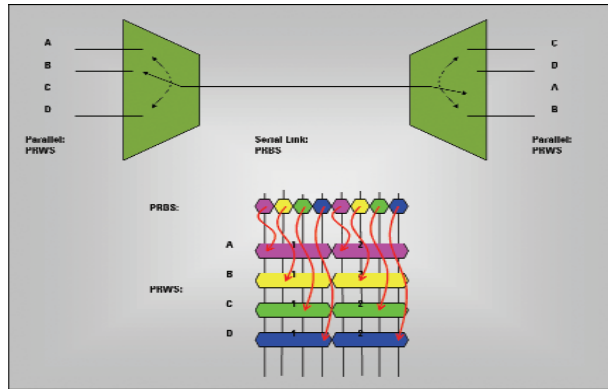
In the case of other kinds of data, synchronization is possible using a detect word. This detect word is available in multiple registers all loaded with one detect word. Once the register has found the correct bit shift, it will define the cycle for error processing.
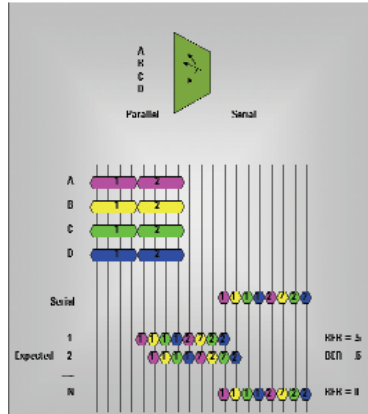
These methods can be enhanced with further optimization of the sampling point: with a timing system, which can adjust the sampling point without having to stop for re-programming of timing values. This can be used for finding the optimum sampling point in the middle of the DUT output signal.

After the synchronization, the BER measurement can be performed. But the trade-off of data synchronization principles means, that the timing relation of input to output data will be lost. So there are no measurements available to measure the latency from input to output.

The second principle will use the capability to move around the sampling point without stopping and re-starting the timing system after re-programming. The 81250 provides such a timing system for the analyzer channels but the range is limited to 10 ns. So this is not a limitation in taking the measurement. As a benefit, the relationship between input and output

Figure 5: PRWS Sequence - pseudo random WORD sequence

Figure 6: Synchronization of Data Cycles

timing is not lost, so latency measurements can be performed.

The Parallel Bit Error Rate Test System

The Agilent 81250 ParBERT is the only Parallel Bit Error Rate solution for 660 Mhz, 1.3 & 2.6 Gbit/s:
• Parallel Bit Error ratio analysis
• Hardware based PRBS up to 2^31-1
• Auto-synchronization: automatic alignment of expected data with data from DUT

• Mixed data: PRBS, PRWS and user-defined data (memory based, up to 8 Meg)
• Handling of multiple frequencies, e.g. Mux/Demux (SERDES)
• Timing measurements after synchronization: change sampling point without stopping the timing system within analyzer
• Handling of differential and low voltage signals e.g. LVDS
• User-interface with 'Standard' and 'Detailed' mode
• Expandability: a choice of channels and frequencies

Product number	Description
E4862A	2.6 Gbit generator front-end
E4863A	2.6 Gbit analyzer front-end
E4864A	1.3 Gbit generator front-end
E4865A	1.3 Gbit analyzer front-end
E4835A	Dual 660 MHz differential analyzer front end
E4832A	660 MHz module
E4861A	2.6 Gbit module
E4805B	Central clock module
E4860A	ParBERT Entry Bundle
E4875A	Software revision 3.0

Besides these, there are Application focussed system configurations:
l • MUX/DEMUX 660 MHz (10Gen/8Ana) E4891A
l • High Speed Bundle 1.3 Gbit/s (2Gen/2Ana) E4892A
l • High Speed Bundle 2.6 Gbit/s (2Gen/2Ana) E4893A

These are easy to order and they are delivered ready to go. The controller has a simple option. Either an embedded or any external PC with a FireWire Interface (E8491A). If additional channels are needed, they also come as simple options.

Synchronization Implementation

The synchronization is done in the 81250-sequencer and module bios software. The PRBS register is implemented in the hardware. The optimization is done, using software located in the hardware module. Figure 7 shows the window from the graphical user interface, which specifies the segment for synchronization when using PRBS.

Loading a short piece of incoming data into the register will synchronize the PRBS. After that it will be clocked for generating further bit stream. The incoming data is now compared to the current incoming data. Any errors can now be identified. Figure 7 also shows how the optimization flow is achieved. For this optimization, you specify a percentage of the cycle depending on how close the final sampling point has to be adjusted to be in the centre of the eye.

MUX Test

For testing the MUX part in the Gigabit Ethernet Chip, a s10 bit wide stimulus for the parallel input is needed as well as a clock channel. This runs with PRWS at 250 Mbit/s. The clock provides a signal of 125 Mhz, so this works with double sampling at the DUT input. The output is a differential PRBS signal at 2.5 Gbit/s.

The 81250 needs two clock groups:
• A clock board (E4805B) with 3 x 660 MHz modules (E4832A) for holding 10 data generators - E4838A (variable transition times) or E4843A (fixed transition times)
• A clock board (E4805B) with 1 Gigabit module (E4861A) with 1 x 2.5 Gbit analyzer front-end (E4863A)
  • A splitter 11667B

The clock is taken from the trigger output of clock board and using the 11667B, the trigger output is provided to the DUT as well as for the second group clock.

The second group clock runs on the external clock provided with the clock from the stimulus group. The frequency needed is 2.5 GHz, which is 20x higher. This factor 20 can be achieved with the frequency multiplier in the external clock input or the channel frequency multiplier or a combination the two. In this example the external clock multiplier is set to 5 and the channel frequency multiplier is set to 4. Figure 8 also shows the window of sequencer programming with the sequencer block for synchronization and the sequencer block for measurement. Note that the actual data segment is PRWS, with $2^{23}-1$ for the DUT input and PRBS of the same polynom as the DUT output. Segments are the same in sync block and measurement block.
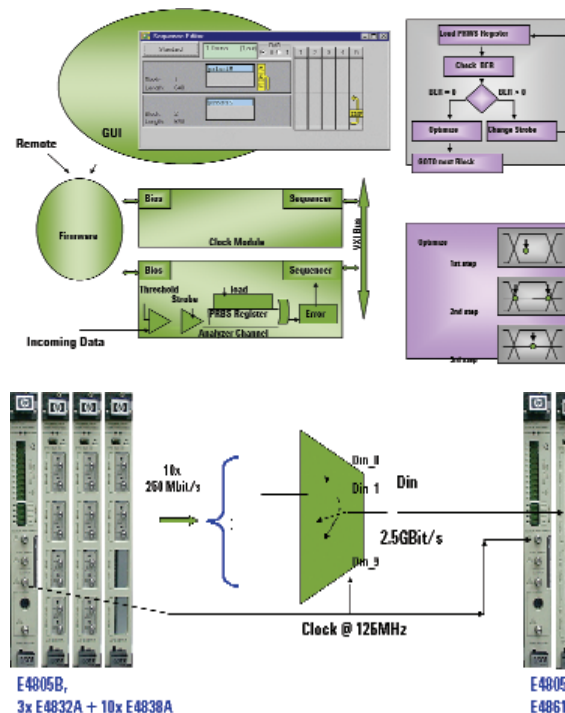

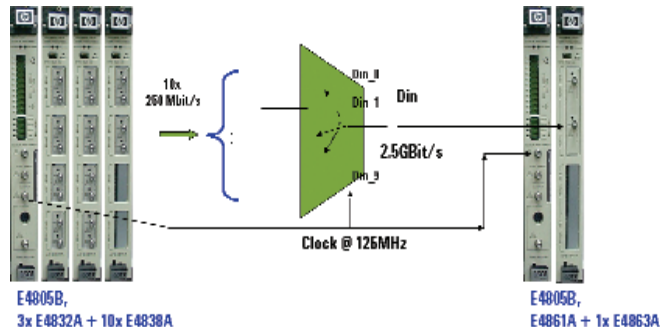**Figure 7: Implementation of Sychronization to PRBS Data (1)**

Figure 8: MUX Test Block diagram

DEMUX Test

For testing the DEMUX part in the Gigabit Ethernet Chip, the opposite configuration is needed:

One 2.5Gbit serial bitstream goes into the analyzer and the analysis is performed with 10 analyzer channels running at 250Mbit/s.

Again, a clock is needed at 125Mhz. The clock group responsible for the serial signal provides this. In addition, a second generator is needed which operates the 125 MHz clock with a data pattern, which repeats 1's 10 times, followed by 0's 10 times. This signal is supplied as a clock once again to the DUT and the analyzer system by means of the splitter.

The following configuration of the Agilent 81250 is recommended:

- A clock board (E4805B) with 1 x Gigabit module (E4861A) with 2 x 2.6Gbit Generator Front-Ends (E4862A)
- A clock board (E4805B) with 3 x 660MHz modules (E4832A) with 10 660MHz Analyzer Front-Ends (as these come as pairs, 5x E4835A is needed)
- A splitter 11667B

The analyzer clock group runs at 250MHz. This is set to the external clock with a frequency multiplier set to the value of 2. This is achieved with a clock given at 125MHz.
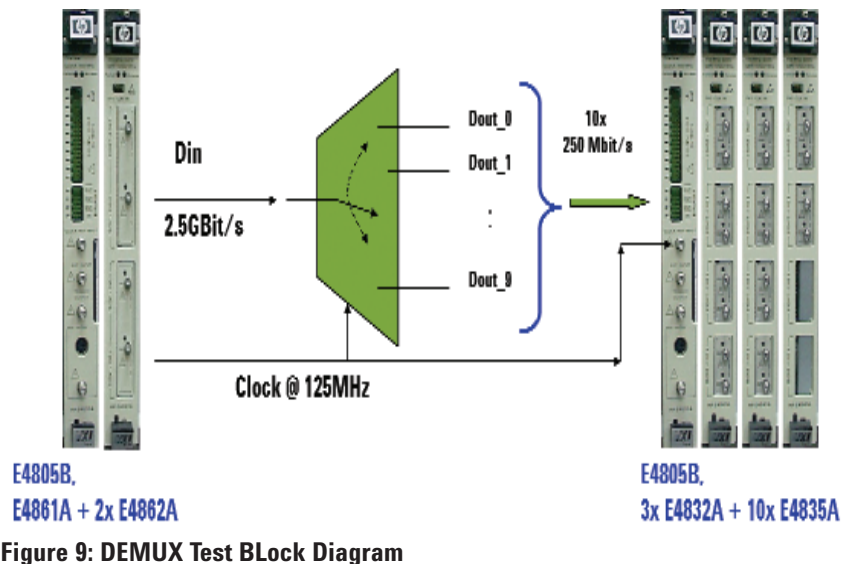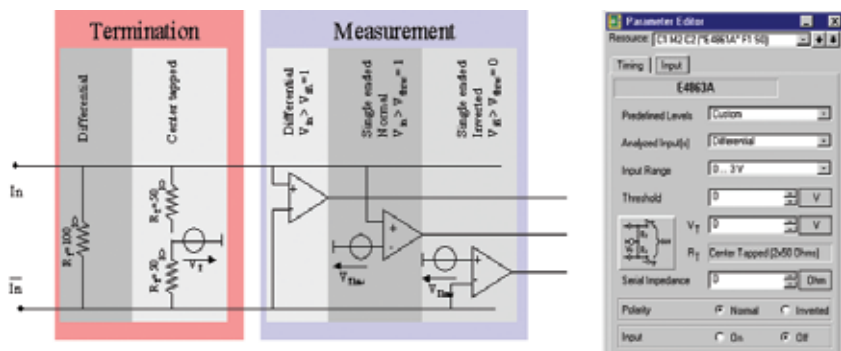

Figure 9: DEMUX Test BLock Diagram

Figure 10: Differential Input architecture

Differential Inputs

The Agilent 81250 offers differential inputs: this is according to the trend that higher speed signals are transmitted with differential techniques. So it provides input and complementary input. This makes the transmission less sensitive to ESD and EMC.

The tolerance to common mode is much better than to single ended signals. Using a differential input it is necessary to select between a differential or a center tapped termination. Differential termination is a 100-Ohm resistor between the two 50-Ohm inputs. Center tapped uses 2 50-Ohm resistors, which are connected to a voltage source, acting as termination voltage.

ECL technology would require center tapped mode with -2V as termination voltage. LVDS would work fine with differential termination.

Measurement mode is independent of termination. There are three comparators, which allow signal comparison as:

• Differential, between input and complementary input
• Single ended normal, normal input vs. threshold
• Single ended inverted, complementary input vs. threshold

The single ended modes are necessary to verify each individual DUT output to be checked for proper function. In case one output gets stuck, the other can still run a proper test with the differential measurement mode. So it is necessary to verify each output against each threshold once.

Differential outputs

Similar issues occur for outputs: If DUT gets faster, it needs more and more complementary signals for driving. This can be achieved by using two channels. However, it would be more economic to use one channel, which provides both signals. It is also important that switching occurs at the same point in time.

Again, the termination model can be selected for outputs. The reason for this is to compensate for the programming values for levels, which would differ with one or other loading.

Characterization

For characterization, the CSC (E4874A) Software can be used. This provides predefined measurement solutions for:
• Eye diagram
• Jitter
• Schmoo plot

SONET OC-192 and SDH STM-64 Testing

Testing at 10Gbit is possible in conjunction with 12 Gbit BER test equipment 76112A.

The 81250 delivers 16 channels with PRWS 2^n-1 at 633Mbit/s. Together with a clock channel, the DUT makes this up to 10Gbits. So the analysis can now be done with 76112 BER tester or communication analyzer.
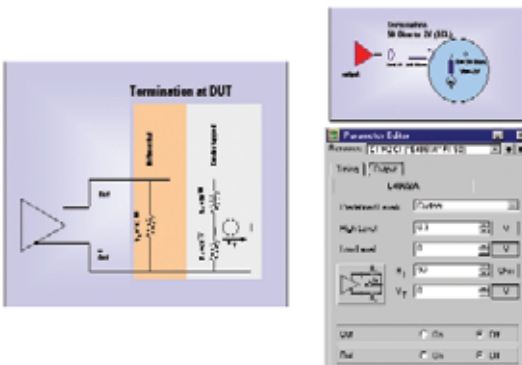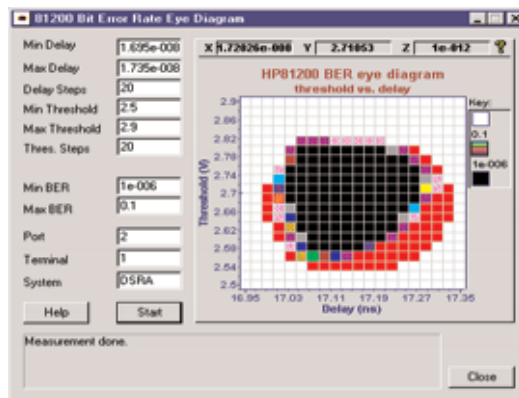

Figure 11: Differential Output architecture

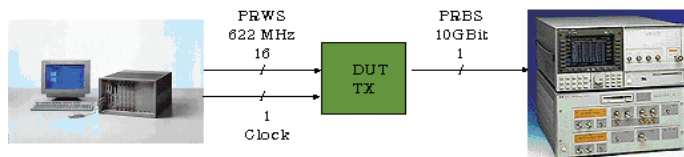**Figure 12: Eye Diagram of a 1.25 Gbit Gigabit Ethernet Transmitter**

Figure 13: Test setup for MUX 622 MHz to 10 Gbit/s

Related literature

	Publication number
• Agilent 81250 Parallel Bit-Error Rate Tester Product Overview	5968-9188E
• Need to test BER? Complete Solutions for high speed digital transmissions Brochure	5968-9250E

For more information, please visit us
www.agilent.com/find/parbert

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